

**WHAT IS CLAIMED IS:**

1           1.       A thin film transistor comprising:  
2           a buffer layer formed on a substrate;  
3           an activation layer formed on said buffer layer; and  
4           a gate insulation layer formed on said substrate including said activation layer,  
5           with said buffer layer having a step formed between a lower part of said activation layer and  
6           a part except said lower part of said activation layer, and said step being a half or less of the  
7           thickness sum of said activation layer and gate insulation layer.

1           2.       The thin film transistor according to claim 1, wherein said buffer layer has a step to  
2           such a degree that thickness of said gate insulation layer is not changed on said side wall of said  
3           buffer layer.

1           3.       The thin film transistor according to claim 1, wherein a thickness of the gate  
2           insulation layer is at least 400 Å when the thickness of SPC polysilicon is 300 Å and step is 350 Å  
3           in the activation layer.

1           4.       The thin film transistor according to claim 1, wherein thickness of the gate insulation  
2           layer is at least 1,000 Å when the thickness of ELA polysilicon is 500 Å and step is 750 Å in the  
3           activation layer.

1           5.     The thin film transistor according to claim 2, wherein a thickness of the gate  
2 insulation layer is 400 Å or more when the thickness of SPC polysilicon is 300 Å and step is 350 Å  
3 in the activation layer.

1           6.     The thin film transistor according to claim 2, wherein thickness of the gate insulation  
2 layer is 1,000 Å or more when the thickness of ELA polysilicon is 500 Å and step is 750 Å in the  
3 activation layer.

1           7.     A method for fabricating a thin film transistor comprising the steps of:  
2 depositing an amorphous silicon layer on a substrate equipped with buffer layer;  
3 forming a polycrystalline silicon layer by crystallizing said amorphous silicon layer;  
4 forming an activation layer by etching said polycrystalline silicon layer;  
5 treating the surface of said activation layer; and  
6 depositing a gate insulation layer on said substrate,  
7 with etching time being controlled in said activation layer forming process and activation  
8 layer surface treatment process so that step between a lower part of gate in the buffer layer and a part  
9 except the lower part of said gate has a step value corresponding to a half or less of the thickness sum  
10 of said activation layer and gate insulation layer.

1           8.     The method for fabricating a thin film transistor according to claim 7, wherein the

2 etching time is controlled so that said buffer layer has a step to such a degree that thickness of said  
3 gate insulation layer is not changed on said side wall of said buffer layer.

1 9. The method for fabricating a thin film transistor according to claim 7, wherein the  
2 etching time is controlled to accommodate said buffer layer having a step corresponding to a half or  
3 less of the thickness sum of the activation layer and gate insulation layer.

1 10. The method for fabricating a thin film transistor according to claim 9, wherein the  
2 etching time is controlled so that said buffer layer has a step to such a degree that thickness of said  
3 gate insulation layer is not changed on said side wall of said buffer layer.

1 11. The method for fabricating a thin film transistor according to claim 7, wherein a  
2 thickness of said gate insulation layer is 400 Å or more when the thickness of SPC polysilicon is 300  
3 Å and step is 350 Å in said activation layer.

1 12. The method for fabricating a thin film transistor according to claim 7, wherein  
2 thickness of said gate insulation layer is 1,000 Å or more when the thickness of ELA polysilicon is  
3 500 Å and step is 750 Å in said activation layer.

1 13. A thin film transistor, comprising:  
2 a buffer layer;

3 an activation layer formed on said buffer layer; and  
4 a gate insulation layer formed on said buffer layer and said activation layer,  
5 with said buffer layer having a step formed between a lower part of said activation layer and  
6 a part except said lower part of said activation layer, and said step being up to a half of the thickness  
7 sum of said activation layer and gate insulation layer.

1 14. The thin film transistor according to claim 13, with said step being controlled  
2 according to said gate insulation layer being deposited to an even thickness on a side wall of said  
3 activation layer.

1 15. The thin film transistor according to claim 13, with a thickness of said gate insulation  
2 layer being at least 400 Å when the thickness of SPC polysilicon is 300 Å and step is 350 Å in said  
3 activation layer.

1 16. The thin film transistor according to claim 13, with a thickness of said gate insulation  
2 layer being at least 1,000 Å when the thickness of ELA polysilicon is 500 Å and step is 750 Å in said  
3 activation layer.

1 17. A method for fabricating a thin film transistor, comprising:  
2 forming a polycrystalline silicon layer;  
3 forming an activation layer by etching said polycrystalline silicon layer;

4           treating the surface of said activation layer; and  
5           depositing a gate insulation layer on said substrate,  
6           with etching time being controlled in the activation layer forming process and activation layer  
7 surface treatment process to accommodate a step between a lower part of a gate in said buffer layer  
8 and a part except the lower part of said gate having a step value corresponding up to a half of the  
9 thickness sum of said activation layer and gate insulation layer.

1           18.     The method for fabricating a thin film transistor according to claim 17, wherein the  
2 etching time is controlled to accommodate said buffer layer including the step to such a degree where  
3 said gate insulation layer is deposited to an even thickness on a side wall of said activation layer.

1           19.     The method for fabricating a thin film transistor according to claim 17, wherein the  
2 etching time is controlled to accommodate said buffer layer having a step corresponding up to half  
3 of the thickness sum of the activation layer and gate insulation layer.

1           20.     The method for fabricating a thin film transistor according to claim 17, wherein a  
2 thickness of said gate insulation layer is at least 400 Å when the thickness of SPC polysilicon is 300  
3 Å and the step is 350 Å in the activation layer or the thickness of said gate insulation layer is at least  
4 1,000 Å when the thickness of ELA polysilicon is 500 Å and the step is 750 Å in said activation  
5 layer.